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CeO_2掺杂对$SrNa_{0.5}Bi_{4.5}Ti_5O_{18}$高温无铅压电陶瓷性能的影响*

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摘 要 用固相合成法制备$SrNa_{0.5}Bi_{4.5}Ti_5O_{18}$ + x%(质量分数) CeO_2 ($SNBTC_x$) 铋层状无铅压电陶瓷, 研究了CeO_2掺杂对$SNBTC_x$陶瓷微观结构和电性能的影响。结果表明, CeO_2掺杂并未改变$SNBTC_x$陶瓷的晶体结构, 所有样品均为单一的铋层状结构陶瓷; CeO_2掺杂没有使$SNBTC_x$陶瓷居里温度发生明显变化, 居里温度均高于560℃; 随着CeO_2掺杂量的增加$SNBTC_x$陶瓷材料的介电常数减小, 但是其介电损耗先增大后减小。当CeO_2掺杂量为0.3%(质量分数)时$SNBTC_{0.03}$陶瓷具有最优电性能: T_c = 567℃, d_{33}=29 pC/N, tanδ=0.015, 且在500℃退极化处理后, 其d_{33}仍保持在22 pC/N以上, 说明$SNBTC_{0.03}$陶瓷可在高温下应用。

关键词 无机非金属材料, 高温压电陶瓷, 铋层状, 压电性能, 温度稳定性

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Effect of CeO_2-doping on Properties of $SrNa_{0.5}Bi_{4.5}Ti_5O_{18}$-based High Temperature Lead-free Piezoelectric Ceramics

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ABSTRACT The lead-free bismuth layer-structured piezoelectric ceramics of $SrNa_{0.5}Bi_{4.5}Ti_5O_{18}$ + x wt.% CeO_2 ($SNBTC_x$) were prepared by solid state reaction and the effect of CeO_2 on the microstructure and electrical properties of the ceramics have been investigated. The result shows that the CeO_2 doping did not alter the crystallographic structure of the ceramics. There were not obvious changes in Curie temperature of the ceramics with the doping of CeO_2, and all the prepared $SNBTC_x$ had high Curie points ($T_c \geqslant$ 560°C). With the increase of CeO_2 contents, the dielectric constant decreased gradually, while the dielectric loss increased firstly and then decreased. Among others, the ceramics $SNBTC_x$ with x=0.3 exhibited the best properties: T_c=567 °C, d_{33}=29 pC/N and tanδ=0.015, besides of which the d_{33} value was still over 22 pC/N after annealing at 500 °C, indicating that the ceramic could be used at high temperature.

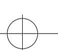
KEY WORDS inorganic nonmetallic materials, high temperature piezoelectric ceramic, bismuth layer-structured, piezoelectric properties, temperature stability

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与铅基及钙钛矿无铅压电陶瓷相比[1-3], 铋层状无铅压电陶瓷有居里温度高、介电常数低、介电损耗小、电阻率高、抗老化性好、高温频率稳定性好等优点, 在高温和高频领域中的应用有很大优势[4, 5]。但是, 铋层状无铅压电陶瓷的压电活性低、矫顽场高和难以极化。因此, 科研工作者们对铋层状无铅压电



陶瓷进行了深入而广泛的研究[6-10]。

掺杂改性是提高压电材料性能的常用手段。Ce是一种变价元素, 能提高材料的电阻率、压电常数和温度稳定性, 常用于钙钛矿与铋层状压电陶瓷的掺杂改性[11-16]。Yan 等[17]用(Li, Ce), (K, Ce)复合置换$CaBi_4Ti_4O_{15}$中A位的Ca, 压电常数d_{33}从7 pC/N增加到20 pC/N。Ma 等[18]也用(Li, Ce)复合掺杂$NaBi_5Ti_5O_{18}$陶瓷, 压电常数d_{33}达到了26.5 pC/N, 退极化温度在500℃时, d_{33}仍保持在19 pC/N。而在众多铋层状无铅压电陶瓷中, $Sr_2Bi_4Ti_5O_{18}$铋层状压电陶瓷具有矫顽场低, 压电活性相对较高的优点, 但是其居里温度仅为296℃, 限制了其在高温领域的应用[9]。

基于此, 本文用CeO_2外掺$SrNa_{0.5}Bi_{4.5}Ti_5O_{18}$(SNBT)陶瓷。通过Ce离子外掺和Na离子内掺的方式, 探索提高$Sr_2Bi_4Ti_5O_{18}$陶瓷居里温度、压电性能及其温度稳定性的新途径。

1 实验方法

以Na_2CO_3(99%)、$SrCO_3$(99%)、Bi_2O_3(99.64%)、TiO_2(99.5%)和CeO_2(99.99%)为原料, 采用固相合成法制备$SrNa_{0.5}Bi_{4.5}Ti_5O_{18}+xCeO_2$($x$ =0, 0.1 , 0.2 , 0.3, 0.4; 质量分数, %)陶瓷。

分别称取原料, 以无水乙醇为球磨介质, 用行星式球磨机(XQM-1L, 南京科析实验仪器研究所)球磨混合原料12 h。将混料取出烘干, 在850℃保温2 h预合成, 然后以去离子水为球磨介质再球磨8 h; 二次球磨后烘干, 再充分研磨后加入10%(质量分数)PVB溶液造粒, 得到流动性好的颗粒。将其在230 MPa压力下干压成型, 得到直径12 mm厚度为1 mm的坯体。

将坯体在800℃保温2 h排塑, 然后在1140℃烧结保温2 h, 得到致密的陶瓷样品; 将烧成后的陶瓷样品打磨、抛光、被敷银电极, 然后在720℃保温20 min烧银, 在180℃硅油内极化。使用MS2671A耐压测试仪, 极化电压为30 kV/cm, 极化时间为20 min。

用X射线衍射仪(D8 Advance)测定$SNBTC_x$陶瓷的物相结构; 用扫描电子显微镜(JSM-6380)观察$SNBTC_x$陶瓷的微观形貌; 用HP4294A型精确阻抗分析仪(Agilent Inc.)测试$SNBTC_x$陶瓷的介电常数和介电损耗; $SNBTC_x$陶瓷的压电常数d_{33}采用准静态d_{33}测量仪YE2730A进行测试。

2 结果和讨论

2.1 相结构分析

图1给出了$SNBTC_x$陶瓷在$2\theta=20^o\sim50^o$范围内的XRD图谱。由图1可以看出, 外掺CeO_2并未引起杂相, 所有样品均具有m=5的单一的正交铋层状结构[9]。这说明, CeO_2离子扩散进入SNBT晶格形成了均一固溶体。由图1B还可以看出, 主峰(1011)出现了向大角度偏移的现象。其原因是, 掺杂的Ce^{4+}半径 (0.092 nm, 配位数为6)小于Sr^{2+}、Na^+、Bi^{3+}的离子半径(0.118, 0.102, 0.103 nm, 配位数为6), 导致晶胞体积减小[19]。这与晶胞参数计算结果相符合。根据Debye Scherrer公式[20], 向大角度偏移说明, 随着CeO_2掺杂量的增大晶粒有长大的趋势。图2给出了

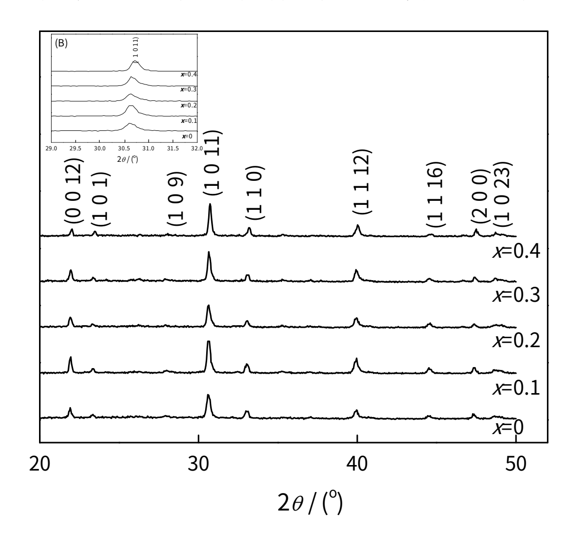


图1 $SNBTC_x$陶瓷样品的XRD图谱

Fig.1 XRD spectra of $SNBTC_x$ ceramics

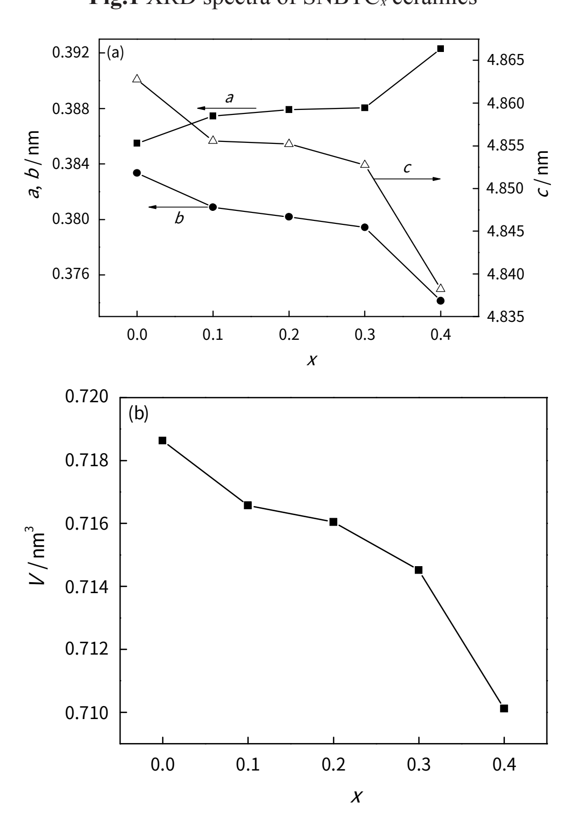


图2 $SNBTC_x$陶瓷的晶胞参数及晶胞体积与x的关系

Fig.2 Relationship between lattice parameters and lattice volume plotted and x

样品晶胞参数随掺杂量x变化曲线图。从图2可以看出, 随着掺杂量的增加晶胞参数a先减小后增大, 晶胞参数c随着x的增加呈现减小的趋势, 晶胞体积V表现出相同的变化, 随着x的增加而减小。晶胞体积变化的原因是, Ce^{4+}扩散进入晶格中取代了部分A位离子, 使晶格产生适度的畸变[21, 22]。在这种情况下电畴也容易运动, 有利于陶瓷的极化提高压电性能[23]。

2.2 微观结构

图3给出了在1140℃保温2h烧结得到的SNBTC$_x$陶瓷表面的SEM照片。从图3可以看出, 所有样品均呈现出典型的层状特征[24, 25]。其原因是, 在烧结过程中晶粒垂直c轴方向的表面具有更低的表面能, 晶粒优先沿着低表面能的平面生长, 导致晶粒沿着a, b轴的生长速率大于沿c轴的生长速率, 最终表现为片状结构[26]。由图3可见, 随着CeO_2掺杂量的增加晶粒尺寸逐渐增大, 晶粒大小趋于均匀, 与CeO_2掺杂量的增加晶界清晰, 且表面也越来越致密, 表明CeO_2的掺杂不仅促进了SNBT陶瓷晶粒生长, 而且促进其致密化, 抑制缺陷的产生, 进而可优化铋层状无铅压电陶瓷的电性能[4, 9]。

2.3 介电性能

图4给出了SNBTC$_x$陶瓷在100 kHz下介电常数和介电损耗随温度的变化关系图谱。从图4可以看出, SNBTC$_x$陶瓷存在的铁电-顺电转变温度, 即居里温度T_c, 随着CeO_2掺杂量的增加SNBTC$_x$陶瓷的居里温度先升高后降低, 但变化幅度较小(560−576℃, 图5)。压电材料居里温度的变化主要受掺杂元素离子半径和电负性的影响: 居里温度随着掺杂元素离子半径降低而升高, 但是随着掺杂元素离子电负性的减小而降低[27]。本文以CeO_2为原材料, 原材料中的Ce离子价态是4+, 但在高温烧结时Ce^{4+}可能转变为Ce^{3+}。Ce^{3+}和Ce^{4+}半径分别为0.101 nm和0.092 nm, 小于Sr^{2+}、Na^{+}、Bi^{3+}的离子半径(0.118, 0.102, 0.103 nm),

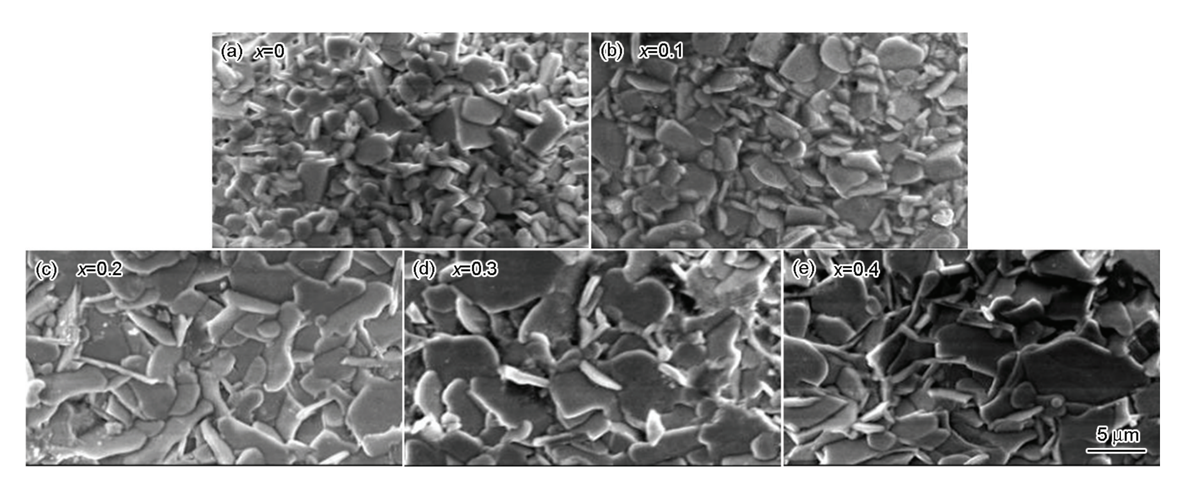
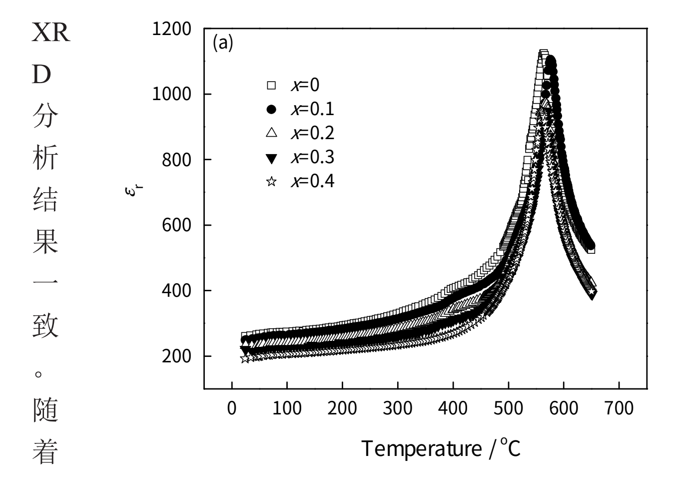


图3 在1140℃保温2 h后SNBTC$_x$陶瓷样品的表面微观形貌
Fig.3 SEM morphologies of SNBTC$_x$ sintered at 1140℃ for 2 h

XRD分析结果一致。随着



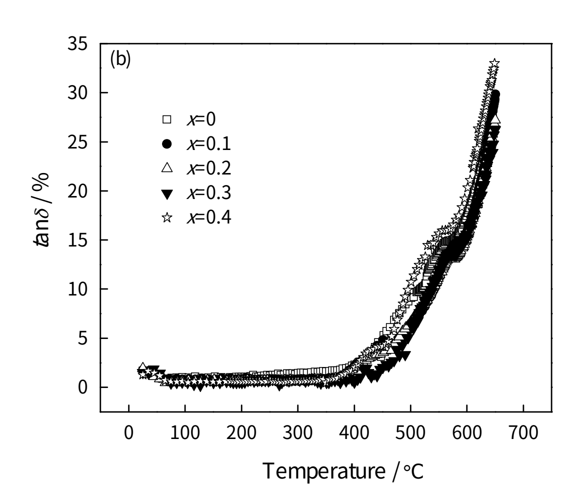


图4 SNBTC$_x$陶瓷样品100 kHz的介电常数和介电损耗与温度的关系
Fig.4 Dielectric constant (a) and dielectric loss tangent (b) of SNBTC$_x$ ceramics as a function of the temperature at 100 kHz

随着CeO_2掺杂量的增加样品的居里温度应该有所升高。另一方面, Ce的电负性(1.12)小于Sr、Na、Bi的电负性(加权平均计算得1.62), 随着CeO_2掺杂量的增加样品的居里温度应有所降低。由图5可以看出, $x\leqslant0.1$时少量CeO_2掺杂主要是离子半径对居里温度影响起主要作用, 导致随着CeO_2掺杂量的增加居里温度升高; $x>0.1$时离子电负性对居里温度影响增强, 随着CeO_2掺杂量的增加居里温度又开始降低。另外, 随着CeO_2掺杂量的增加SNBTC$_x$陶瓷的介电常数减小。根据Shannon[19]有效离子半径, 在配位数为6时Ce^{3+}和Ce^{4+}离子半径分别为0.101 nm和0.092 nm, 与A位的离子半径接近。因此在理论上, Ce^{3+}和Ce^{4+}进入A位取代Sr^{2+}、Na^+、Bi^{3+}, 电价不平衡而产生A空位。根据软性掺杂与硬性掺杂理论, A空位的产生为软性掺杂效应, 其压电常数和介电常数会升高; 但若产生过多的A空位就会使晶格畸变过大, 造成介电常数降低[28]。另外, Ce^{3+}和Ce^{4+}离子半径小于Sr^{2+}、Na^+、Bi^{3+}的离子半径, 小半径的离子掺杂使离子极化减小[29], 也降低其介电常数。由图4b可见, 在室温到450℃时该材料的介电损耗一直低于5%左右, 特别是样品x=0.3, 在温度上升到500℃时其损耗仍低于5%。这表明, 该材料具有良好的温度稳定性。

2.4 压电性能及温度稳定性分析

图6给出了SNBTC$_x$陶瓷室温时的压电常数d_{33}及其随退火温度的变化曲线。由图6可知, 室温时SNBTC$_x$陶瓷的压电常数d_{33}随着掺杂量的增加先增大后减小。当x=0.3时压电常数d_{33}达到29 pC/N, 高于$SrBi_4Ti_4O_{15}$[30]、$SrCaBi_4Ti_5O_{18}$[9], $SrBi_2Nb_2O_9$[31], $CaBi_4Ti_4O_{15}$[32], $Bi_4Ti_3O_{12}$[33]等其它高温铋层状压电陶瓷。说明适量外掺CeO_2可显著提高铋层状压电陶瓷的压电活性, 因为外掺CeO_2后铋层状压电陶瓷会

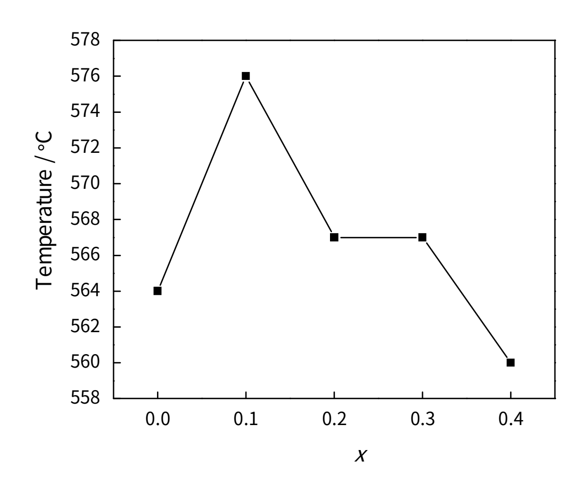


图5 SNBTC$_x$陶瓷的居里温度与x的关系

Fig.5 Influence of x on Curie temperature of the SNBTC$_x$ ceramics

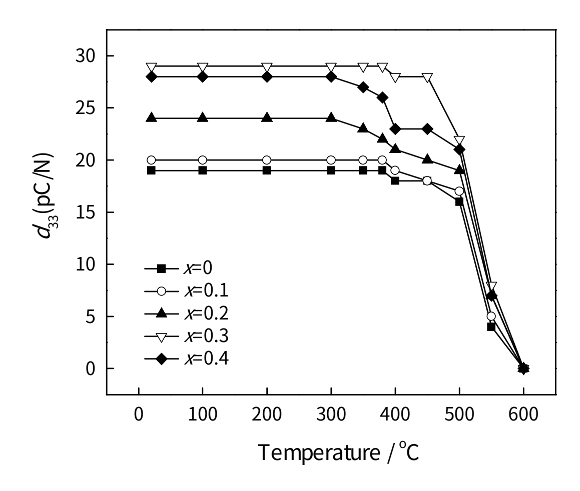


图6 SNBTC$_x$陶瓷的室温d_{33}及随退火温度的变化

Fig.6 Influence of annealing temperature on d_{33} of the SNBTC$_x$ ceramics

产生适度的空位和晶格畸变, 使畴壁在外场作用下转向变得容易, 材料能够充分极化, 进而提高了其压电性能[23, 34, 35]。由图6还可以看出, SNBTC$_x$陶瓷压电常数d_{33}随着退火温度的升高表现平稳, 接近400℃时所有样品的压电性能才有所降低。其原因是, 适量CeO_2掺杂引起SNBTC$_x$陶瓷离子键键能增加, 离子之间的结合能更高, 需要更高的能量才能使其发生破坏, 因而提高了SNBTC$_x$陶瓷的温度稳定性。温度稳定性表现最为突出的是掺杂量x=0.3的陶瓷材料, 在退火温度为500℃时退极化时间为30 min, d_{33}仍然保持在22 pC/N以上。这说明, SNBTC$_{0.3}$陶瓷具有更好的温度稳定性, 适合于制备高温环境中应用的压电器件。

3 结　论

采用固相法可制备出SNBTC$_x$铋层状无铅压电陶瓷。所有陶瓷均为纯的5层铋层状结构陶瓷, 陶瓷的晶粒为片状, 随着CeO_2掺杂量的增加晶粒逐渐增大, 结构愈发致密。当CeO_2掺杂量为0.3时压电常数d_{33}高于其它高温铋层状压电陶瓷, 达到29 pC/N; SNBTC$_x$铋层状无铅压电陶瓷具有高的居里温度(T_c = 567℃)和低的介电损耗($\tan\delta$ < 5%); 当退火温度为500℃时压电常数d_{33}仍保持在22 pC/N以上, 表明SNBTC$_{0.3}$无铅陶瓷具有良好的温度稳定性, 适用于制备高温高频压电器件。

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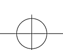
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